What is Claimed is:

1. A semiconductor integrated circuit device which has plural circuit blocks coupled in series for signal transmission and whose whole operation is controlled by a clock signal,

wherein the plural circuit blocks include a first circuit block that receives input signals in response to a first timing signal based on the clock signal, and a second circuit block that forms output signals in response to a second timing signal based on the clock signal, and

wherein a time difference between the first timing signal and the second timing signal is set to a period of a non-integral multiple of the cycle of the clock signal.

2. The semiconductor integrated circuit device according to claim 1,

wherein time from the receipt of an input signal in the first circuit block to the output of a signal formed in the second circuit block is set to an integral multiple of the cycle of the clock signal.

3. The semiconductor integrated circuit device according to claim 1,

wherein a timing signal forming circuit is provided which forms the first timing signal and the second timing signal, based on the clock signal, and

wherein the timing signal forming circuit has a program element and includes a delay circuit for adjusting the time difference between the first timing signal and the second timing signal by the program element.

4. The semiconductor integrated circuit device according to claim 3, wherein the program element is comprised of fuse devices.

5. The semiconductor integrated circuit device according to claim 4,

wherein at least one of the plural circuit blocks has a circuit operation setting element and the setting of circuit operations thereof is changeable depending on the circuit operation setting element, and

wherein the program element in the delay circuit and the circuit operation setting element in the circuit block are configured with the same device configuration as each other.

6. The semiconductor integrated circuit

device according to claim 5,

wherein the second circuit block is comprised of a random access memory having a defect relieving circuit, and

wherein the program element in the delay circuit and a setting element for holding defect relief information in the defect relieving circuit in the second circuit block are configured with the same device configuration as each other.

7. The semiconductor integrated circuit device according to claim 6,

wherein the random access memory is comprised of a synchronous memory that forms output after a period exceeding plural times a clock signal cycle from the start of access thereto.

8. The semiconductor integrated circuit device according to claim 7,

wherein the synchronous memory is comprised of a memory whose memory cells are dynamic memory cells.

9. The semiconductor integrated circuit device according to claim 5,

wherein the program element in the delay circuit and the setting element for holding defect

relief information in the defect relieving circuit in the second circuit block are provided adjacently to each other.

10. The semiconductor integrated circuit device according to claim 9,

wherein the program element in the delay circuit and the setting element for holding defect relief information in the defect relieving circuit in the second circuit block are nearly linearly juxtaposed.

11. A semiconductor integrated circuit device which has a signal input point, a signal output point, and plural circuit blocks provided in series between the signal input point and the signal output point and in which the timings of a signal input operation from the signal input point, a signal output operation at the signal output point, and a signal transmission operation among the plural circuit blocks are respectively controlled by timing signals,

wherein, when the clock signal cycle is T1, the total of signal response periods of individual circuit blocks of the plural circuit blocks is T2, and the ratio T2/T1 between T1 and T2 is $n+\alpha$ (n is

an integer and α is a positive number equal to or less than 1), a signal response period from the signal input point to the signal output point is set to n+1 times the clock signal cycle T1.

12. A semiconductor integrated circuit device which has plural circuit blocks coupled in series for signal transmission and whose whole operation is controlled by a clock signal,

wherein the plural circuit blocks include a first circuit block and a second circuit block that receive input signals in response to a first timing signal based on the clock signal, and a third circuit block that forms output signals in response to a second timing signal based on the clock signal,

wherein, in a signal transmission system, the third circuit block is provided between the first circuit block and the second circuit block, and

wherein a time difference between the first timing signal and the second timing signal is set to a period of a non-integral multiple of the cycle of the clock signal.

13. The semiconductor integrated circuit device according to claim 12,

wherein the third circuit block includes a

local timing signal generating circuit that generates a third timing signal within the block, based on the second timing signal, and a time difference between the second timing signal and the third timing signal is a non-integral multiple of the cycle of the clock signal.

14. The semiconductor integrated circuit device according to claim 13,

wherein the local timing signal forming circuit has a program element and includes a delay circuit for adjusting the time difference between the second timing signal and the third timing signal by the program element.

15. The semiconductor integrated circuit device according to claim 13,

wherein the first circuit blocks and the second circuit block each include a latch circuit that gets input signals to the respective circuit blocks, based on the first timing signal, and the third circuit block includes a latch circuit that gets input signals to the third circuit block, based on the second timing signal.

16. The semiconductor integrated circuit device according to claim 12,

wherein, in the signal transmission system consisting of the first circuit block, the third circuit block, and the second circuit block coupled in series for signal transmission, one or two or more fourth circuit blocks are provided in parallel with the third circuit block.

17. The semiconductor integrated circuit device according to claim 16,

wherein the third circuit block and the fourth circuit block have the same circuit configuration, and a signal selecting means for selectively transmitting one of output signals corresponding to the circuit blocks is provided in the second circuit block.

18. The semiconductor integrated circuit device according to claim 12,

wherein a timing signal forming circuit is provided which forms the first timing signal and the second timing signal, based on the clock signal, and

wherein the timing signal forming circuit has a program element and includes a delay circuit for adjusting the time difference between the first timing signal and the second timing signal by the

program element.

19. The semiconductor integrated circuit device according to claim 12,

wherein there are provided two external terminals through which the clock signal is inputted, and a clock buffer circuit which receives a differential clock signal inputted to the two external terminals and generates a single-phase clock signal.

20. The semiconductor integrated circuit device according to Claim 11,

wherein said plural circuit blocks include a first circuit block and a second circuit block,

wherein said first circuit block receives a signal input in accordance with a first timing signal,

wherein said second circuit block outputs a signal output in accordance with a second timing signal,

wherein said first and second timing signals are controlled by said clock signal.

21. The semiconductor integrated circuit device according to Claim 20, further comprising:

a timing generating circuit which generates said first and second timing signals in accordance with said clock signal;

a plurality of DRAM macro cells;

a read and write buffer; and

an address decoder,

wherein said timing generating circuit includes a delay circuit which is programmable.

22. The semiconductor integrated circuit device according to Claim 21,

wherein said time difference between said first and second timing signals is other than a multiple cycle of said clock signal.

23. The semiconductor integrated circuit device according to Claim 21, further comprising:

a redundancy address setting circuit including fuses, and

wherein said timing generating circuit includes fuses.